Automated Sun Tracking in Unidirection with Solar Cell or PV Panel

Thwe Thwe Zin

Abstract

Automated sun tracking circuit for PV arrays are constructed, tested and explained in this research. The sun tracking circuit is constructed using CMOS ICs (4070, 4027), 555 timers, transistors and LDRs. Only one stepper motor is used. Unlike tracking circuits using microcontrollers, our circuit need not be programmed and it is less expensive and easier to maintain.

Introduction

As we know that sun rises in the East and sets in the West. During its motion there is a circular path. The means to follow the movement of the sun is called solar tracking. As solar cells produce electricity when sun light falls on it, the solar cell can sense the position of the sun. By using this property solar tracking system is constructed. Maximum condition is always maintained by turning the motor. The motor moves the solar panel. Using electronic components necessary decision are made.

1. BACKGROUND THEORY

1.1 Unipolar Stepper Motor

There are several designs of stepper motors. The four-phase unipolar stepper motor is two motors sandwiched together. Each motor is composed of two windings. Wires connect to each of the four windings of the motor pair, so there are eight wires coming from the motor. The common from the windings are ganged together, which reduces the wire count to five or six instead of eight.

In operation, the common wires of a unipolar stepper are attached to the positive side of the power supply. Each winding is energized by grounding it to the power supply for a short time. The motor shaft turns a fraction of a revolution each time a winding is energized. For the shaft to turn properly, the windings must be energized in sequence. e.g; energize wires 1, 2, 3 and 4 in sequence and the motor turns clockwise.

Assistant Lecturer, Dr, Department of Physics, Kyaukse University

The wave step sequence is the basic actuation technique of unipolar stepper motors. It actuates two windings at once in an on-on / off-off four step sequence. This actuation sequence increases the driving power of the motor. The phasing sequence is provided by means a port following a four-bit binary sequence: 1010, 0110, 0101, 1001.

Results and Discussions

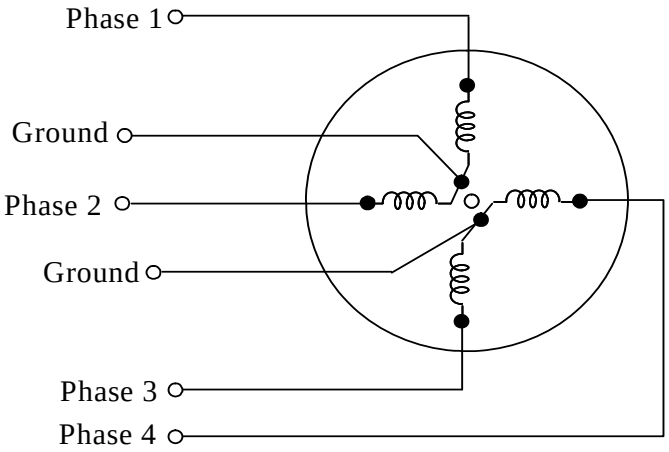


Fig. 1. The wiring diagram of the unipolar stepper.

STEP	PHASE 1	PHASE 2	PHASE 3	PHASE 4
1	■		■	
2		■	■	
3		■		■
4	■			■

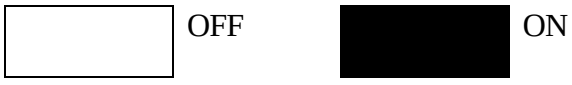


Fig. 2. The enhanced on-on/off-off four-step sequence of a unipolar stepper motor.

1.2 The 555 Timer

The 555 timer is one of the most versatile linear integrated circuits designed. It may be used in many different configuration to satisfy a wide variety of applications include monostable and an astable multivibrators, voltage-controlled oscillators, timers and wave generators.

- The 555 timer has the following features.
- supply voltage from 5V to 18V.
- adjustable duty cycle, timing from microseconds through hours
- high current output capability (200 mA)
- can be TTL compatable
- temperature stability of 50 ppm (parts per million)

The input include threshold, trigger, control voltage, discharge, and reset. External capacitors and resistors are used to configure the timer as an astable multivibrator, which will produce a train of pulses as an oscillator.

1.3 The 555 as an astable multivibrator

In this mode of operation, the 555 circuit is known as an astable multivibrator or rectangular wave oscillator. Another common name for it is a free-running oscillator, since the circuit requires no external trigger signal for its operation.

When the 555 is connected as an astable oscillator, the input sees a waveform that is set by the charging and discharging of the capacitor. Since the capacitor will continue to charge and discharge as long as an input voltage signal is applied, the output will continue to provide a square wave (on/off) output waveform.

1.4 Astable operation

The operation of the 555 timer in the astable mode may be described by three phases. The first phase (power-up phase) occurs only one time during power-up. The charge and discharge phases occur alternately after the power-up phase.

The charging time, Tc is

$$T_C = 0.69 (R_A + R_B)C$$

The discharging time, T_D is

$$T_D = 0.69 R_B C$$

The period of the resulting rectangular wave is

$$T_{rectangle} = T_C + T_D$$

The frequency is

$$f_{rectangle} = 1/T_{rectangle}$$
$$= 1.45/[(R_A+2R_B)C]$$

duty cycle is

$$\text{duty cycle} = (T_C/T_{rectangle}) \times 100\%$$
$$= (R_A + R_B)/(R_A + 2R_B) \times 100\%$$

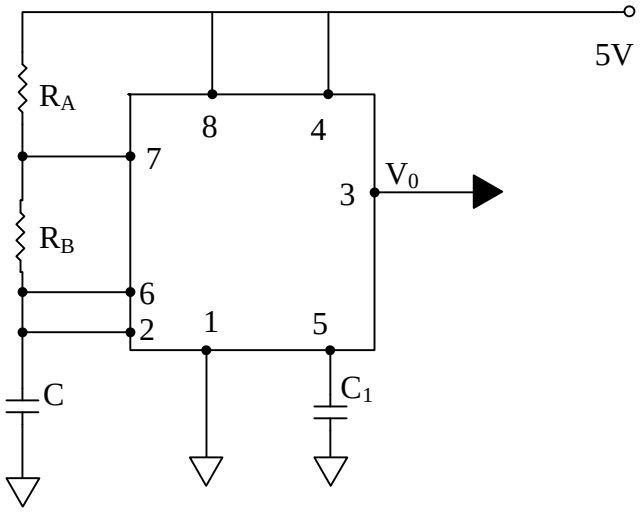


Fig. 3. The 555 Timer with Astable Mutivibrator Circuit.

1.5 4027 JK Flip-flop

The HEF4027B is a dual JK flip-flop which is edge-triggered and features independent set direct (S_D), clear direct (C_D), clock (CP) inputs and outputs (O, $\overline{O}$). Data is accepted when CP is LOW, and transferred to the output on the positive-going edge of the clock. The active HIGH asynchronous clear-direct (C_D) and set-direct (S_D) are independent and override the J, K, and CP inputs. The outputs are buffered for best system performance. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

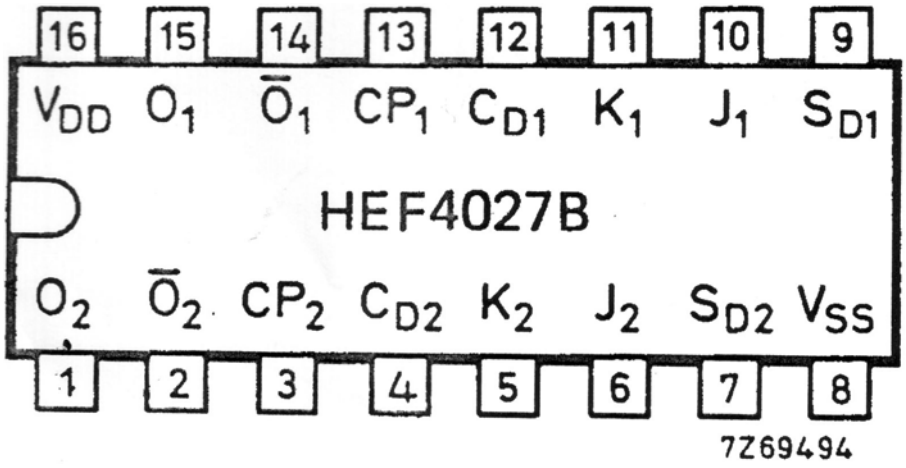
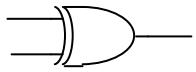


Fig. 4. Pinning Diagram of 4027 IC

1.6 4070 XOR Gate

A gate whose output is high only when the input word has odd parity.



Truth Table for two input XOR Gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

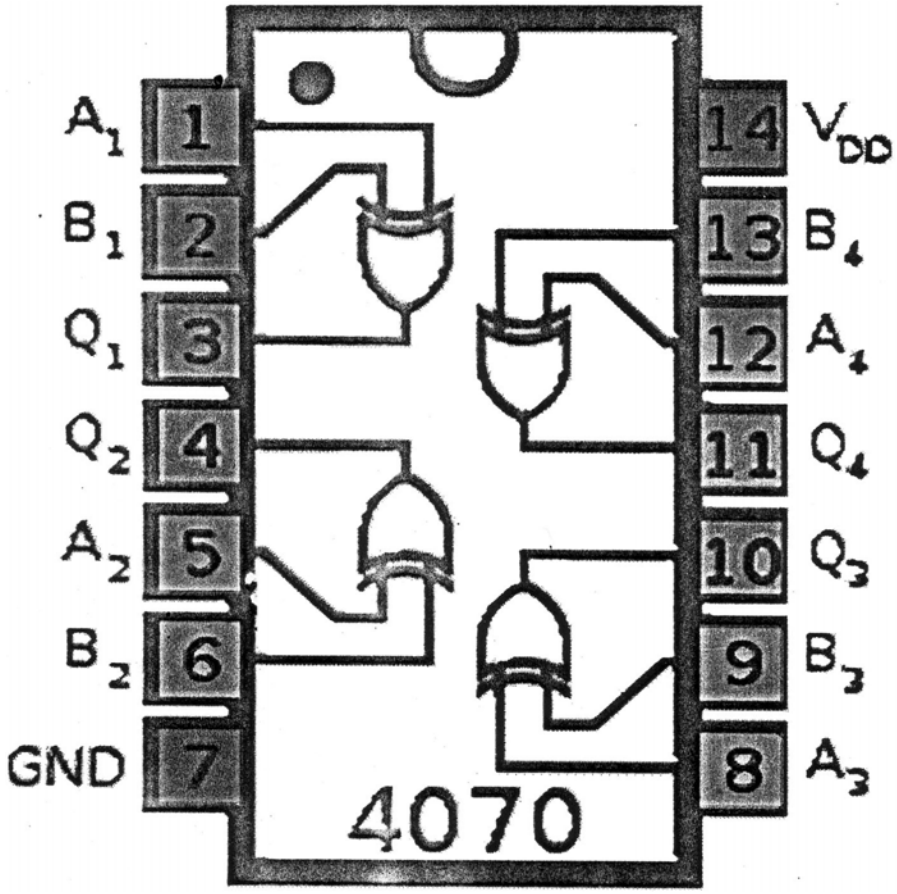


Fig. 5. Functional Diagram of 4070 IC

1.7 Construction of Sun Tracking System for PV Array

The constructed sun tracking system consists of light sensor circuit and stepper motor drive circuit.

The light sensor circuit is constructed by using transistor, light dependent resistors (LDRs) and preset resistors as shown in Fig 3.6.

The sun tracker uses a combination of three photoresistors R5, R3 and R2, to ensure that the circuit will follow the sun during the day, but not look for it at night. Photoresistor cells, R5, R3 and R2 have a value of 160Ω in full sunlight and 4880Ω in the shade, that is not absolutely critical. R5 is mounted in a "well" with a narrow slit so that sunlight falls upon it only when the photoresistor is pointed directly at the sun. When that occurs, R5's resistance drops. That photoresistor and PR2 form a voltage divider at the base of the Darlington transistor, Q1. When R5's resistance is low, Q1 will be kept off.

When the sun swings a little westward, R5 will no longer be in sunlight, causing its resistance to go up, which raises the base voltage of Q1 and turns that Darlington on. That in turn closes the relay, K1, providing current to the drive motor, putting R5 in direct sunlight again; Q1's base voltage then drops and the tracker stops. Photoresistor R3 is mounted on the outside of the well so that it receives a wide angle of sunlight when the sun is shining, R3' resistance is low, keeping Q2 turned off, and allowing the tracker to act as described, without interference. But if the sun "slips" behind a cloud, R3's resistance goes high producing a forward bias on the base of Q2. That turns the transistor on and sinks the base of Q1 to near ground so that Q1 then remains off. That immobilizes the tracker drive; that also keeps the drive shut down in the dark of night.

Photoresistor R2, is the dawn sensor. It is mounted on the back of the sun tracker. When the tracker stop at sunset, pointing toward the west, R2 is pointing toward the east. When the sun rises the following morning and shines on R2, its resistance goes low, turning Q2 off and allowing Q1's base to go high. That presents current to the relay and therefore to the drive motor, causing the tracker to swing around to the east.

The stepper motor drive circuit is designed and constructed using NE 555 timer IC, X OR gate IC, JK flip-flop IC, resistors, diodes and power transistors. The NE 555 timer IC (IC 1) is connected as an oscillator. The oscillation frequency is controlled by the resistor R7, preset resistor PR3 and capacitor C_1. Therefore the preset resistor PR 3 can be used to adjust the frequency output of the oscillator obtained from the pin 3 of IC 1 and it is routed to the clock input pins (pin 3 and pin 13) of the dual JK flip-flop IC (IC 3). The J and K inputs of the two

JK flip-flops are tied together to form as T (toggle) flip-flops. The outputs of the flip-flop change its logic states with the rising edges of clock signals.

Initially the logic states of flip-flop outputs (Pin 15, Pin 14, Pin 1 and Pin 2) are assumed to be '1010'. This means that the Q output of IC 3a (pin 15) is a logic '1' state and $\overline{Q}$ output of IC 3b (pin 2) is at logic '0' state. The pin 15 and pin 2 of the JK flip-flop is fed back to the inputs of the two input X OR gate (IC 2b). Therefore the output of the X OR gate (IC 2b) is in logic '1' state. Two inputs of the X OR gate (IC 2a) is tied together and connected with + 12V power supply (logic '1' state). So IC 2a behaves as an invertor gate and its output is always logic '0' state. The output of X OR gate (IC 2a) is connected to pin 8 of IC 2c and the output of IC 2b is connected to pin 9 of IC 2c. The output of the X OR gate (IC 2c) is, therefore, in the logic '1' state. The output is then put to the JK inputs of the flip-flop (IC 3a). The outputs of the JK flip-flop will change (or toggle) its logic state when the leading edge of the clock signal is received. Therefore the logic states at pin 15 and pin 14 will be changed to logic '0' and logic '1', respectively. At the sametime, the logic states at the inputs of the X OR gate (IC 2d) are both at logic '1' state. Therefore, the output of the IC 2d is at logic '1' state The output of the IC 2d is fed to the JK inputs of the flip-flop, IC 3b. Therefore the outputs pin 1 and pin 2 will hold their previous logic '1' and logic '0' state. The four outputs of two JK flip-flops after receiving the first clock pulse will be '0110'. At that condition, the inputs of the IC 2b will be changed into logic '0' states and the output be comes logic '0' state. By tracing the logic states through four X OR gates and two JK flip-flops, one can easily see that the outputs of JK flip-flops changed its logic states in the following four bit binary sequence (1010, 0110, 0101, 1001, 1010, . . . etc).

The outputs of the JK flip-flops are used to drive power transistors. 4 Tranfistors, Q3 through Q 6 used in the stepper motor drive circuit are Darlington pair power transistors and they are used as transistor switches. The transistor is 'ON' when the logic '1' state is received at its base input through the current limiting resistor. The collectors of the transistor are connected with the stepper motor coils. The common terminal of the stepper motor coils is connected to +12V power supply via the relay. The emitters of the transistors are connected to ground. When the transistor is 'ON' the collector of that transistor is grounded. This also grounded the corresponding stepper motor coil. Therefore the current flows from the +12V power supply to the stepper motor coil and collector emitter junction to the ground. In this way the stepper motor is drived for a gain sequence of steps.

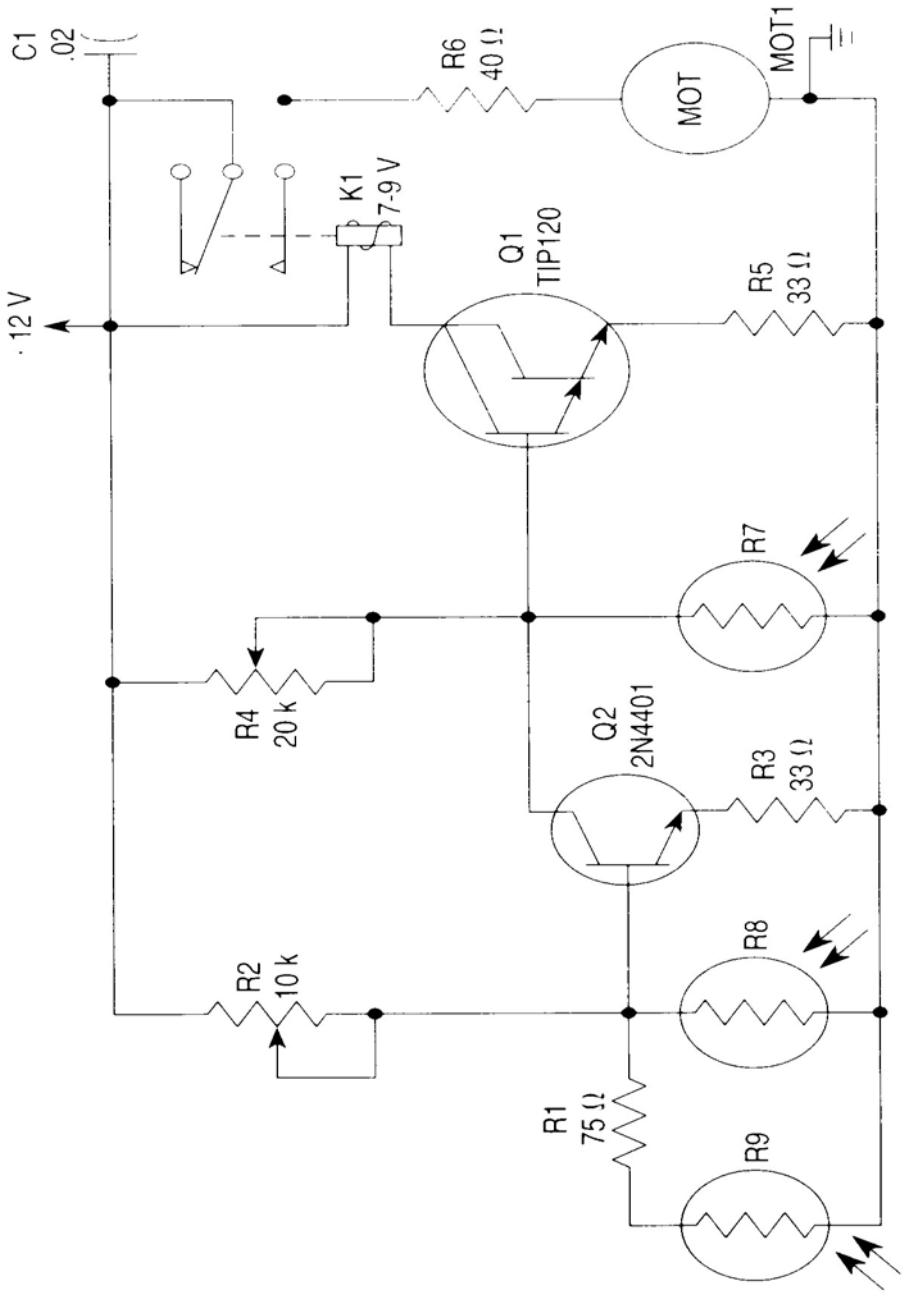


Fig. 6. Schematic Diagram of Light Sensor Circuit

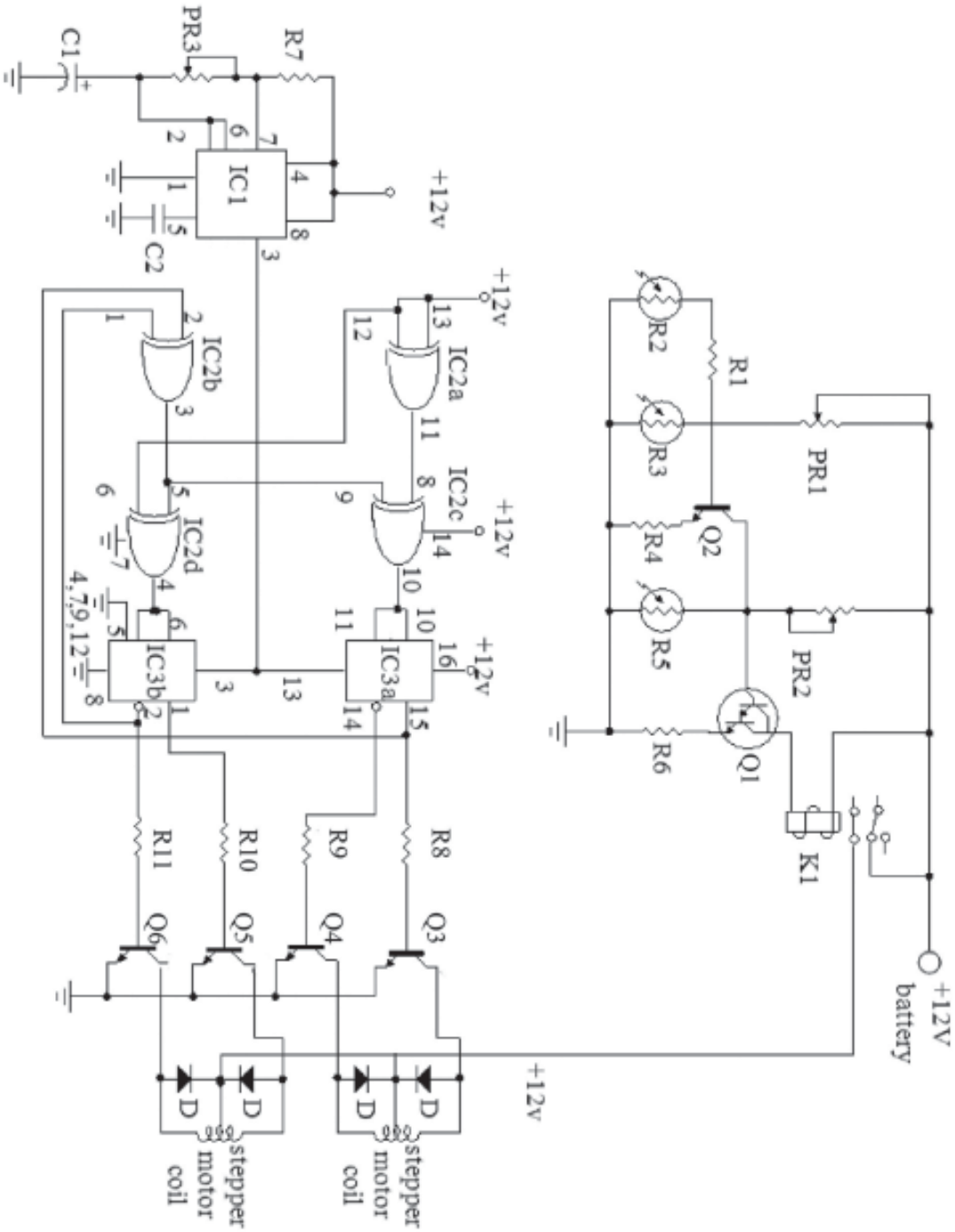


Fig. 7. Complete Circuit Diagram of Sun Tracking System for PV Array

RESULTS AND DISCUSSION

This paper presents the implementation of an electronic instrument for solar energy utilization purpose. The system consists of two main sections, light sensor section and solar panel tracking section. The solar panel tracking section is designed to update the orientation of solar panel. The operation of solar tracking section is based on the behavior of light dependent resistor (LDR). The changes in resistances of LDRs cause the shift in biasing points of transistors in this solar panel tracking section. In this work, a solar energy utilization system is constructed. The solar panel tracking section is responsible for keeping the orientation of the solar panel in direct facing to sun. This section is designed to update the orientation of the solar panel when the solar radiation falling upon the sensor LDRs, cause the biasing point shifting. The presently constructed tracking circuit uses three sensor LDRs; two for front sensing and one for back sensing. The tracking can be made manually as well as automatically.

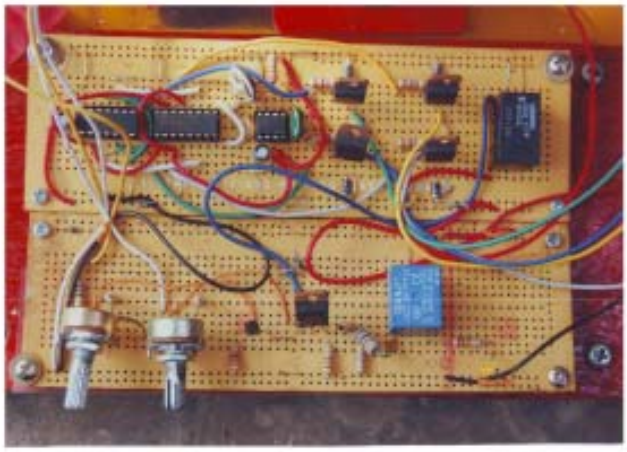


Fig. 8. The Photograph for only Circuit Diagram of Sun Tracking System

Fig. 9. The Photograph for Complete Diagram of Sun Tracking System

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